IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 09/639,422, filed August 14, 2000, ~~pending~~ now U.S. Patent 6,597,066, issued July 22, 2003, which is a divisional of application Serial No. 09/518,293, filed March 3, 2000, now U.S. Patent 6,287,942, issued September 11, 2001, which is a continuation of application Serial No. 09/244,733, filed February 5, 1999, now U.S. Patent 6,084,288, issued July 4, 2000, which is continuation of application Serial No. 08/910,613, filed August 13, 1997, now U.S. Patent 5,903,044, issued May 11, 1999, which is a continuation of application Serial No. 08/614,178, filed March 12, 1996, now U.S. Patent 5,682,065, issued October 28, 1997.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] Referring initially to drawing FIG. 5, a portion of a silicon substrate wafer 10 is shown having portions of two semiconductor chips 12 formed thereon, each semiconductor chip 12 having, in turn, bond pads 14 thereon, passivation layers 18 thereon, circuitry 20 therein, and street areas 22 located between the semiconductor chips 12 formed on the wafer 10. Initially, while the semiconductor chips 12 are in the form of a wafer 10, the active circuitry side of the semiconductor chips 12, i.e., the top or first side of the wafer 10, is coated with ~~a layer 30 of~~ suitable etchable glass layer 30 of sufficient thickness to cover the wafer 10 in its entirety including the street areas 22 formed between the adjacent semiconductor chips 12 on the wafer 10 while maintaining the surface of the wafer 10 in a substantially planar state. The glass layer 30 of etchable glass may be added to the wafer 10 by any suitable well known technique, such as spin coating, dip or flow coating. It is preferable that the etchable glass coating be a type of glass that cures at a relatively low temperature, such as curing at a temperature generally less than six hundred degrees Centigrade (600° C) and is easily etched in subsequent etching processes. Such types of etchable glasses are well known and may be selected depending upon processing convenience during manufacture.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] Referring to drawing FIG. 8, after the removal of the resist coating, the next step in the method of the present invention is to apply a suitable etchable glass coating 40 to the bottom or second side of the semiconductor chips 12 formed on the wafer 10 to uniformly coat the bottom or second sides of the semiconductor chips 12 and fill the etched portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10. The etchable glass coating 40 may be of any suitable material and applied by any suitable manner as described hereinbefore. After the application of the glass coating 40 of etchable glass to semiconductor chips 12, the semiconductor chips 12 effectively remain in the form of a wafer 10 by the glass layer 30 and the glass coating 40 reforming the wafer 10 by filling the street areas 22 previously etched between the semiconductor chips 12 and coating both the top and bottom, first and second sides, of the wafer 10.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] Referring to drawing FIG. 9, the next step of the method of the present invention comprises applying a suitable resist material (not shown) to the glass layer 30 and etching the glass layer 30 through to expose the bond pads 14 of the semiconductor chips 12. In this manner, the bond pads 14 of the individual semiconductor chips 12 are exposed to have suitable connections made thereto.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] Referring to drawing FIGs. 12A, 12B and 12C, the steps of the method of the present invention of making a substantially fully hermetically sealed semiconductor ~~wafer~~ chip ~~10~~ 12 are shown in flow process form corresponding to such steps being previously described with reference to drawing FIGs. 5-10. In a flow process form, the method of the present invention of making a substantially fully hermetically sealed semiconductor chip 12 generally comprises the following sixteen (16) steps. The method of the present invention substantially begins by forming the desired individual semiconductor chips 12 on a wafer 10. If

desired, the individual semiconductor chips 12 are tested for functionality while on the wafer 10. This step is shown as being optional.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

[0042] The fourth step of the present invention comprises another optional step where the thickness of the wafer 10 is thinned to provide an even planar surface. The wafer 10 may be thinned from the bottom or second side thereof by any suitable means, such as ~~chemical-~~ chemical-mechanical planarization, mechanical abrading, etc. While such thinning is desired, it may not be necessary if the wafer 10 has a sufficiently planar lower surface. Also, if the wafer 10 is sufficiently thin to be etched by conventional etching techniques in the steps of the present invention described hereinafter, the wafer 10 need not be thinned.

Please replace paragraph number **[0054]** with the following rewritten paragraph:

[0054] As the sixteenth step of the method of the present invention, portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10 are sawed through at locations 50 in the street areas 22 so that glass layer 30 and glass coating 40 are maintained on the edges of each semiconductor chip 12 and the active circuitry (top or first) side of the semiconductor chip 12 and the bottom (second side) of the semiconductor chip 12, thereby substantially hermetically sealing the semiconductor chip 12 in glass while the bond pads 14 are substantially hermetically sealed by the metal coating forming the desired circuits 16 connected thereto. In this manner a plurality of semiconductor chips 12 have been formed with each semiconductor chip 12 being substantially fully hermetically sealed on each side thereof and on each edge thereof and the bond pads 14 being substantially hermetically sealed by the metal coating forming the circuits 16 to prevent environmental corrosion thereof without the use of a separate package. By using the method of the present invention to substantially fully hermetically seal the semiconductor chip 12, without the use of a separate package, the semiconductor chip 12 of the present invention is of minimum size and occupies a minimum volume. Also, the semiconductor chip 12 formed by the method of the present invention has a

desired configuration of circuitry connecting the bond pads 14 of the semiconductor chip 12 to a desired connector configuration which may include conventional lead frames 60 or lead-~~over~~-over-chip frames. If connected to lead frames, the semiconductor chip 12 of the present invention which is fully hermetically sealed in glass layer 30 and glass coating 40 may be subsequently packaged in suitable plastic materials in a conventional manner for further protection from damage. If desired, since the semiconductor chips 12 are substantially fully hermetically sealed by glass layer 30, having the desired circuitry 16 thereon, and glass coating 40, the semiconductor chips 12 may be directly inserted into mating connectors which match the circuitry formed on the semiconductor chips 12.